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TITLE: UNIVERSAL ASYNCHRONOUS BOUNDARY MODULE INVENTORS: PARAS SHAH AND PRASHANTHA KALLURAYA

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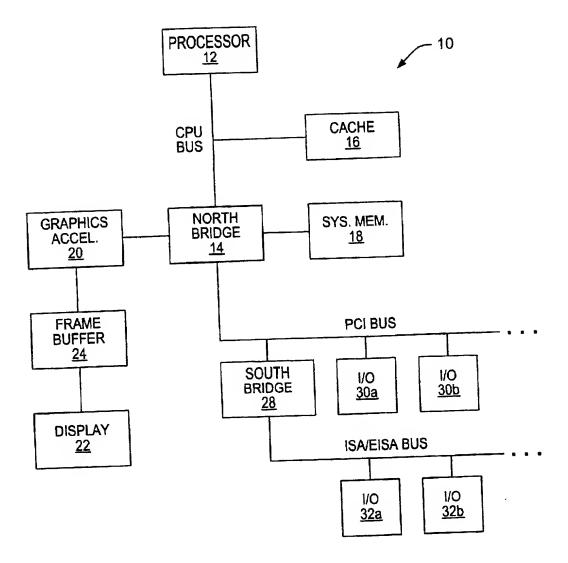


FIG. 1

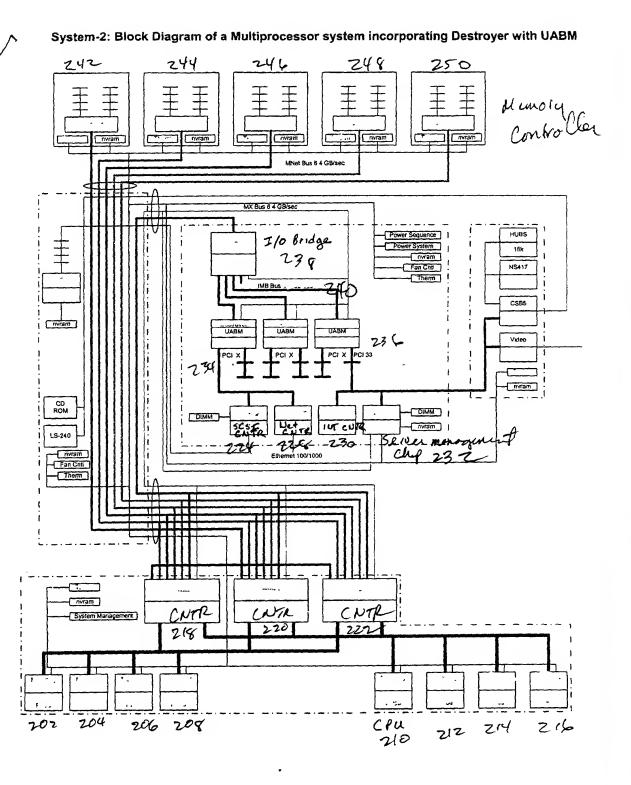
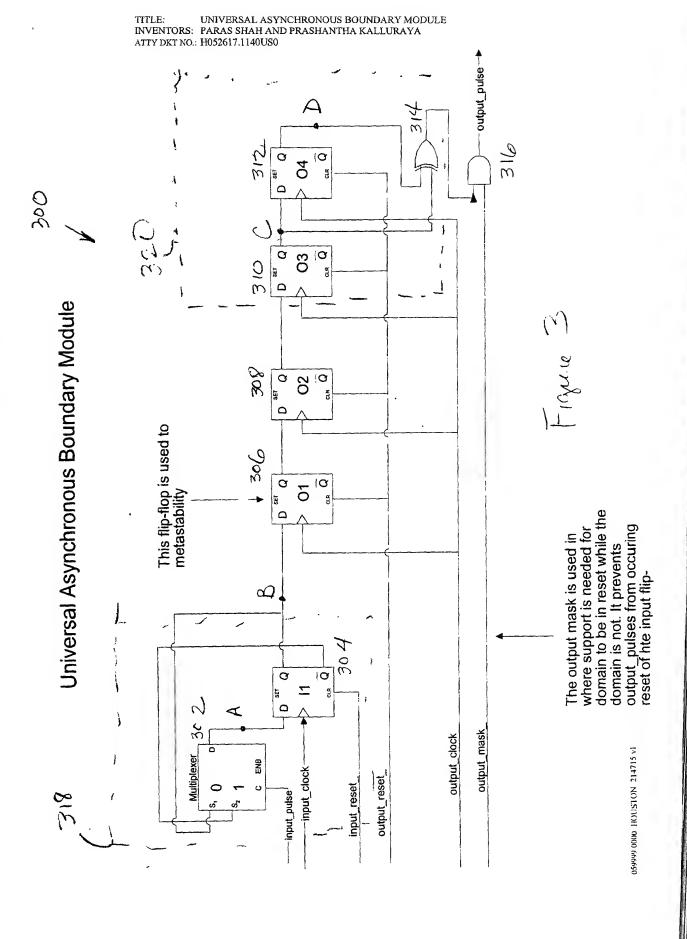


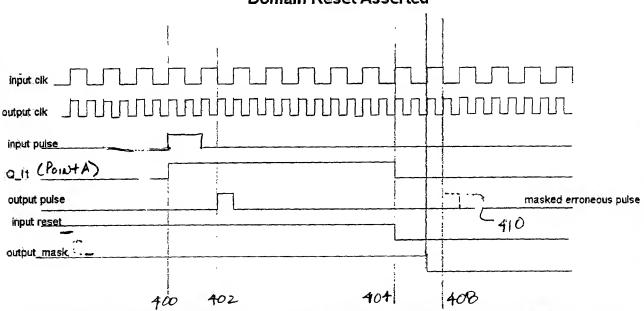
Figure 2



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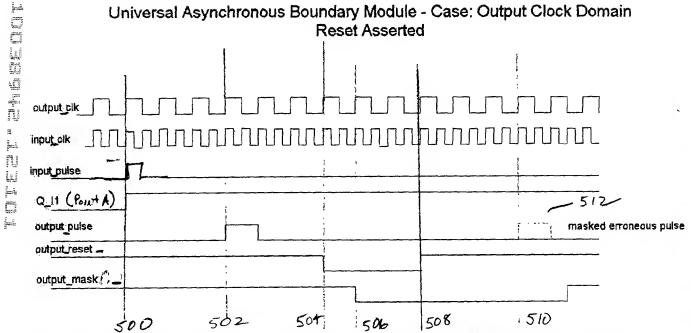
Note: Asserting the output mask prevents possible occurance of erroneous pulse when input clock domain's reset (input reset) is asserted

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Figure 4

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Note: Asserting the output mask prevents possible occurance of erroneous pulse when output clock domain's reset (output reset) is asserted

Figure 5

